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; Date : 28 September 1999

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; File : pllcon.asm

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; Hardware : ADuC824

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; Description : Demonstrates that the CPU can run at different

; speeds determined by the CD bits in the PLLCON SFR.

; 2 to the power of CD (a 3 bit number), is the divider

; ratio that determines the clock frequency at which

; the CPU will run. (CD=0 =>fcore=12.58MHz,

; CD=7 => fcore=98.3kHz)

;

; The program turns on and off the LED approx every

; 70,000 machine cycles. With the higher frequency

; (CD=0 =>fcore=12.58MHz) the LED toggles at about

; 16Hz. By pressing the INT0 button the CD bit is

; incremented (CD=1 =>fcore=6.3MHz) and the LED will

; toggle at half the frequency as before. At the

; minimum frequency (CD=7, fcore=700kHz) the LED

; toggles at 0.125Hz. By pressing INT0 button again

; CD rolls over to 0 again and the LED

; toggles at 16Hz again.

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$MOD824 ; Use 8052&ADuC824 predefined symbols

LED EQU P3.4 ; P3.4 drives red LED on eval board

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; BEGINNING OF CODE

CSEG

ORG 0000h

JMP MAIN ; jump to main program

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; INTERRUPT VECTOR SPACE

ORG 0003h ; (INT0 ISR)

CPL LED ; complemant LED to indicate INT0

; press.

MOV R2,#136 ; reinitialise R7 and R6 so that

MOV R3,#256 ; after interrupt the full delay

; loop is completed

MOV A, PLLCON ; Only increment CD bits of PLLCON

INC A ; Rollover to PLLCON = xxxxx000b (fmax)

ANL A, #07h ; after PLLCON = xxxxx111b (fmin)

MOV PLLCON, A ; where the x's are 1's and 0's as rqd

RETI

;====================================================================

ORG 0060H ; Start code at address above interrupts

MAIN:

MOV PLLCON, #00H

SETB IT0

SETB EX0 ; enable ext int INT0

; (button on eval board)

SETB EA ; enable interrupts

BLINK: CPL LED

CALL DELAY ; wait for 70,000 machine cycles

; =66ms at fmax

; =8.5s at fmin

JMP BLINK

;====================================================================

DELAY: ; This loop delays the program for 70,000

; (approx) machine cycles, corresponding

; to a delay of 66ms at fmax and 8.4s

; at fmin

MOV R2,#136 ; 136 \* 256 \* 1.907us = 66ms

DLY1: MOV R3,#256 ;

DJNZ R3,$ ; sit here for 256 x 2 x machine

; cycle time (=488us @ fmax)

DJNZ R2,DLY1 ; repeat 136 times (=66ms total @ fmax)

RET

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END